REMARKS

Summary

Claims 1-7, 48, 52-54 and 58-60 were pending and Claims 1-4, 7, 48, 52-54 and 58-60 were rejected in the present Office action; Claims 5 and 6 were objected to. Claim 48 has been amended. No new matter has been added. The Applicants have considered the references and the arguments made by the Examiner and respectfully traverse the rejections on the basis that a *prima facie* case of anticipation has not been set forth.

Objections

With respect to Claim 48, the Applicants respectfully traverse the objection to the use of "a plurality of the conductive pairs" in line 12. The Examiner's comments are noted, however, the Applicants respectfully submit that such an extensive change to the structure of the claim is not necessary. Claim 48 has, however, been amended to eliminate an apparent redundant reference to the more than one of the conductive rod pairs that are arranged as recited.

As many of the words and phrases of a patent claim have acquired a special meaning in the art of claim drafting and interpretation, the Applicants have made use of these forms in making the metes and bounds of the claim as clear as possible to a person of skill in the relevant art, and respectfully request that the objection be withdrawn.

With respect to Claims 5 and 6, the Examiner has objected to the claims as being dependent on a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. The Applicant's express appreciation to the Examiner for this indication of allowable subject matter, but respectfully decline to make the suggested amendments as, as argued below, the base claims are allowable.

Claim Rejections

35 U.S.C. 102(b)

Claims 1-4, 7, 48, 52-54 and 58-60 were rejected under 35 U.S.C. 102(b) as being anticipated by Hernandez (US RE 35,064; "Hernandez")). The reference is a reissue of US 5,065,284.

Claim 1 recites, *inter alia*, first conductive rods connected to the second conductive layer and extending to the first conductive layer, and chip capacitors connected to the first conductive rods and arranged in a lattice.

In addition to the arguments presented in the previous response, which are reiterated and amplified below, the Applicants respectfully suggest that the Examiner's characterization of FIG. 13 of the reference is not read on by the present Claim 1, and a *prima facie* case of anticipation has not been made out.

In order to better understand the Examiner's description of FIG. 13 of the reference, and for the purpose of this traverse only, the following table associates reference numbers found in Hernandez with features of the FIG. 13, so that the differing terminology may be better discussed. The association between the terms of the claim and the terms used by Hernandez is for convenience only, and to demonstrate that, even adopting the Examiner's interpretation, a *prima facie* case of anticipation has not been made out.

Ref Designator	**Hernandez description**	**Citation**	**Examiner's usage**
132	Inner ground plane	Col. 7, lines 6-7	First conductive layer
128	Outer voltage plane	Col, 7, line 6	Second conductive layer (98)
130	Outer voltage plane	Col. 7. line 6	
124, 126	Flexible dielectric sheet	Col. 7, line 4	Lattice
92, 94	Insulative layer	Col. 7, lines 7-8	Dielectric layer

96	Flexible dielectric sheet	Col. 6, line 10	
102	Planar layer of spaced ceramic chips	Col. 6, lines 10-11	Chip capacitors
120, 118	Vias in circuit board 90B	Col. 6, line 65-66	Conductive Rods

As best understood, the Applicants now paraphrase the Examiner's description of FIG. 13 of Hernandez as:

> A second conducting layer (98 or 128) separated from the lattice (124) by a first dielectric layer (92). The second conductive layer (98 or 128) separated from the first conductive layer (132); first conductive rods (120) comprising plated vias passing through first dielectric layer(92) and the first dielectric layer is disposed between the first (132) and second (98) conductive layers, connected to the second conductive layer (92) and extending to the first conductive layer (132); and chip capacitors (102) arrayed over substantially an entire area of the first conductive layer (132), connecting the first conductive rods to the first conductive layer, and arranged in a lattice (124).

Arguendo, accepting this description, the Examiner asserts that the first conductive rod (120) (for example the leftmost rod in FIG. 13) passes through the first dielectric layer (92) and connects to the second conductive layer (98 or 128) and extends to the first conductive layer (136).

The Applicants respectfully submit that the first conductive rod (120) passes though the second conductive layer (98 or 128) and extends to the first conductive layer (138). Using the Examiner's terminology, none of the other rods in FIG. 13 are read on by Claim 1. Therefore, not all of the elements and limitations of Claim 1, and the arrangement thereof, are found in the reference, and a *prima facie* case of anticipation has not been made out. Lindemann Machinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir 1984) (citing Connell v. Sears Roebuck & Co. 722 F.2d 1542 220 USPQ 193 (Fed. Cir. 1983))

The Applicants respectfully traverse the Examiner's characterization of element 102 [not labeled, but shown in FIG. 9] in FIG. 13 as a "chip capacitor". At col. 6 line 10-11, the reference describes element 102 as "spaced ceramic chips". Hernandez differentiates this element at col. 6, lines 38-49, where element 102 from being a chip capacitor, as an advantage of the invention is said to be that it "eliminate[es] the need for discrete decoupling capacitors" (col. 6, lines 19-21). Moreover, an isolated ceramic chip is not a capacitor *per se*, as will be appreciated by a person of ordinary skill in the art. This point is further addressed below. As such, the reference does not teach the arrangement of Claim 1, and all of the elements thereof, and a *prima facie* case of anticipation has not been made out.

In the Examiner's response to arguments, the issue of whether the reference teaches discrete capacitors such as the chip capacitors of Claim 1 was addressed, and the statement of Hernandez that the invention "eliminates the need for discrete capacitors" has been discounted. The Applicants respectfully disagree. Hernandez teaches that the invention eliminates the need for discrete capacitors. The Examiner has mischaracterized layer 124 or chips 102 as "discrete capacitors" (Id.). These elements cannot be "discrete capacitors", as the ceramic chips are an essential feature of Hernandez, and Hernandez explicitly disclaims that discrete capacitors are needed.

Claims 2-7, 48, 52-54, and 58-60 were rejected for the reasons traversed above, and are allowable for at least the same reasons, or as claims dependent on an allowable claim.

Moreover, with respect to independent Claim 48, the Examiner asserts that the reference shows a plurality of conductive rod pairs 118-120 disposed in a rectangular periodic pattern. At best FIG. 13 shows a linear (not rectangular) pattern of dissimilar rods, two of which the Examiner may choose to call a pair, but since the rods are equally spaced from each other, the limitation in Claim 48 of "adjacent", describing a pair of rods, is not found. Moreover, the figures of the reference do not reasonably suggest that a periodic pattern of pairs of rods, where the rods are as described in Claim 48, is formed.

Claims 48, 52-54 and 58 60 were rejected under 35 U.S.C. 102(b) as being anticipated by McKinzie III (US 6,476,771; "McKinzie"). FIG. 9 of the reference is used as showing the elements described by the Examiner. The Applicants respectfully traverse the Examiner's characterization of elements 911 and 914 as "chip capacitors" or even as capacitors, based on a purported association in the reference with "capacitive frequency surface (FSS) capacitors." The term "capacitive frequency selective surface (FSS)" is used to describe element 102 in Fig. 1 (col. 3, lines 29-31), and is not found elsewhere in the specification, nor is the word "capacitor" found in the phrase. The Examiner's terminology describing element 102, or elements 911 and 914, as a "chip capacitor" is not supported by the specification, and the Examiner makes no attempt to explain why a reasonable person of ordinary skill in the art would accept the proffered term. As such, similarly to the discussion of the first reference, the Examiner has not shown that all of the elements and limitations of the present claims are taught in a single reference, and thus a *prima facie* case of anticipation has not been made out.

Claims 48, 52-54 and 58 60 were rejected for the reasons traversed above, and are allowable for at least the same reasons, or as claims dependent on an allowable claim.

The Examiner contends that, during examination, terms in the claims may be given their broadest reasonable interpretation. The Applicants respectfully submit that the actual requirement is somewhat more restricted. "The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." (*In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed.Cir. 1999)). MPEP 2111, second paragraph. (emphasis added). The Examiner cites "Dorland's Illustrated Medical Dictionary" as an authoritative source of a definition to be used a person of ordinary skill in the art in understanding of the claim.

As an electrical engineer is not a healthcare professional, it would not be a reasonable interpretation of a claim, even in the broadest sense permitted, to use a definition of a term prepared for the use healthcare professional in lieu of that which any electrical engineer would find in a specialized treatise or dictionary. Even in a standard dictionary such as the Merriam-Webster's Collegiate Dictionary (10th Edition), where a

capacitor is defined as "a device giving capacitance and usu. consisting of conducting plates or foils separated by thin layers of dielectric...." Thus while a dielectric, such as a ceramic chip, may contribute to the capacitive effect of the device, a dielectric layer *per se* is not a capacitor.

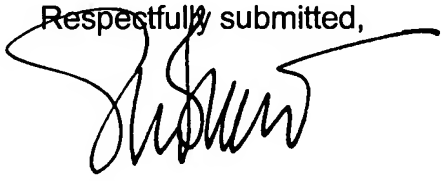
The Applicant therefore traverses the rejections on the basis that the Examiner has not used the term "capacitor" as a person of ordinary skill in the art (electrical engineering) would have done in understanding the claim and that, as such, a *prima facie* case of anticipation has not been made out.

Conclusion

Claims 1-7, 48, 53-54 and 58-60 are pending. Claim 48 has been amended. For at lest the reasons given above, the Applicants respectfully submit that the application is in condition for allowance.

The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application.

Respectfully submitted,



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